Ultra-fast, Low-Power Integrated Circuits in a Scaled Submicron HBT IC Technology

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Abstract

We have developed fast, dense, and low-power integrated circuits using a new scaled IC process. We have fabricated HBT's of 0.3 μm^2 emitter and circuit metalization pitch of 4 μm to reduce power and compact the chip size. Submicron HBT's exhibited f_T of over 160 GHz. We have demonstrated a number of circuits including a low-power comparator test chip clocked at 40 GHz.

I. Introduction

Heterojunction bipolar transistor (HBT) based integrated circuits have shown potential for LSI levels of integration. Power consumption will be a major limitation of high-speed HBT integrated circuits unless transistors are scaled down to submicron dimensions.

In this work, We have demonstrated fast, dense, and low-power integrated circuits using a newly developed scaled HBT IC technology on InP substrate. We have been able to achieve low circuit power consumption by reducing the HBT emitter dimensions to a size of 0.5 μm^2. This is a significant reduction in the emitter area of transistors achieved in our baseline IC technology [1]-[2]. To achieve chip area compaction, we have reduced the interconnect metalization pitch from the original 8 μm in our baseline process down to 4 μm. The submicron HBT's exhibited f_T values of greater than 160 GHz and dc current gain of greater than 50. Using this new process, we have demonstrated circuits including a clock & data recovery chip and a comparator test chip clocking at 40 GHz frequency. Each comparator cell comprising 21 transistors consumed approximately 25 mW dc power from a single 3.2 V negative supply. The

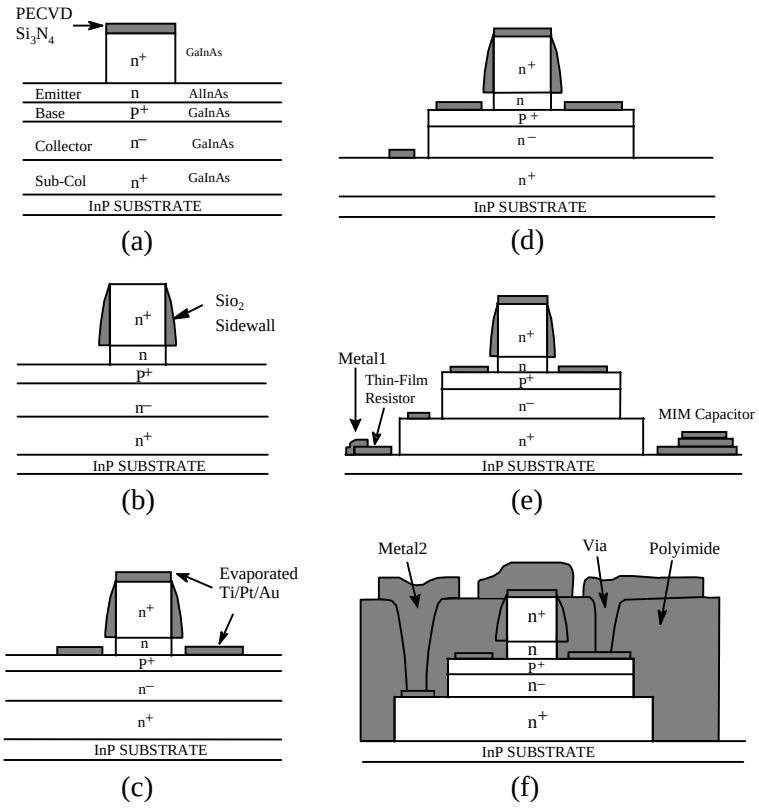

Fig. 1 Schematic cross-sectional view of the submicron HBT IC process

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comparator is a key building block and speed limiter of parallel or flash architecture analog-to-digital converters (ADC). Parallel ADC's require 2^n comparators for n-bit accuracy.

II. Fabrication Technology:

A schematic cross-sectional view of the scaled HBT IC process is shown in Fig. 1. In this process we define very fine emitter geometries into a thin layer of silicon nitride which acts as a mask to remove the n^+ emitter cap layer by reactive ion etching (RIE) techniques (Fig. 1a). Subsequently we form a sidewall by depositing SiO_2 and reomowing it using RIE. Subsequently this SiO_2 sidewall forms overhangs shown in Fig. 1b when we remove the n-emitter by wet chemical etching. A single metalization step then defines both the emitter and base ohmic contacts (Fig. 1c). Base-collector mesa, collector ohmic and isolation mesa follows as shown in figures 1d and 1e. At this point in the process we fabricate resistors, capacitors and first interconnect metal layer (Fig. 1e). Final stages of the process is shown in Fig. 1f where we planarize the wafer with polyimide, etch via holes by RIE, and pattern second metalization layer for global circuit interconnection.

Using this new process we have been able to successfully fabricate HBT's with emitters as small as 0.3 μm^2. This is more than a factor of 10 reduction in the emitter area of transistors compared to our baseline minimum geometry HBT which was 2x2 μm^2.

III. Transistor Characteristics:

I-V characteristics of a typical 0.5 μm^2 HBT is shown in Fig. 2 exhibiting a dc current gain of over 50 for a submicron transistor. Furthermore, this device can carry a collector current density of greater than 10^6 A/cm^2 as seen in Fig. 2. This is due to a minimal self-heating in a device with such a small emitter geometry.

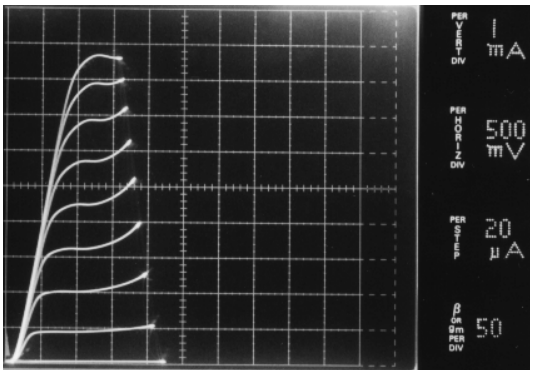

Fig. 2 I-V characteristics of a 0.5 μm^2 emitter HBT.

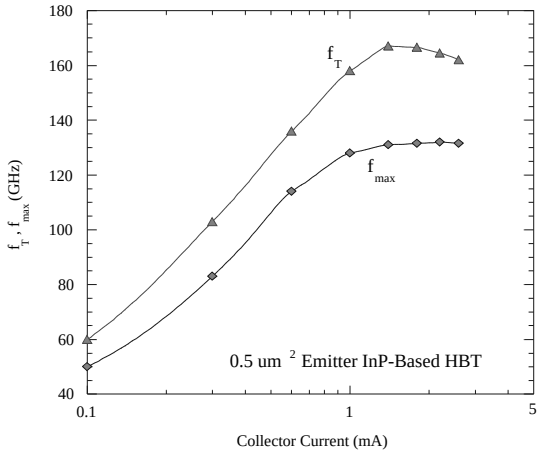

Fig. 3 RF performance of 0.5 μm^2 HBT

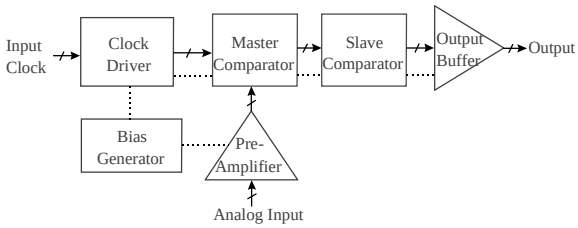

Fig. 4 Block diagram of comparator test chip implemented with scaled HBT process (90 HBTs, mostly 0.5 μm^2 emitter)

The RF performance of the scaled HBT is shown in Fig. 3 where we have plotted the unity

gain cutoff frequency, f_T and maximum frequency of oscillation, f_{max} as a function of collector current. These measurements were done at a collector-emitter voltage of 1.25 V. We measured higher values of f_T and f_{max} at V_{CE} of 1.5 and 1.75 V. As seen in Fig. 3, the transistor exhibited an RF performance of greater than 40 GHz at 100 μA of collector current while the peak values of f_T and f_{max} occurred at around 1 mA.

IV. Circuit Implementation:

Using this new process we have demonstrated a comparator test chip comprising two cascaded master-slave comparators, a pre-amplifier, a bias generator, a clock driver and an output buffer - a total of 90 transistors. A block diagram of the test chip is shown in Fig. 4. All the circuitry were designed in a fully differential architecture for maximum speed advantage. The master-slave comparators (comprising a total of four latch states) were driven by opposite phases of the clock. This improved ability of comparators to resolve small differential inputs [3]. The pre-amplifier and the cascaded master-slave comparator set form the key building block of parallel (also known as flash) architecture analog to digital converters.

A chip photograph of the fabricated comparator test chip is shown in Fig. 5. The chip was layed out for on-wafer characterization with signal pads adjacent to ground connections. The fabrication process was optimized to significantly reduce the metalization pitch (metal width plus metal-to-metal spacing) from 8 μm in our baseline process down to 4 μm. Correspondingly, the via sizes had to be scaled down to submicron dimensions. The reduction in the metalization pitch has a significant effect on compacting the chip size. In complex IC's (such as ADC's), this can potentially reduce the chip size by a factor of 4. The size of the comparator test chip reported here was reduced by a factor of approximately 3 (due to reduction in the metalization pitch and the transistor sizes), compared to a similar layout in our baseline process. This reduction in the chip size will dramatically increase the circuit yield.

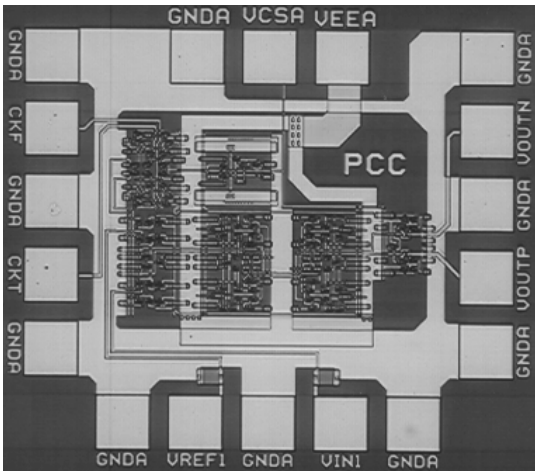

Fig. 5 Die photo of fabricated comparator test chip using scaled 0.5 μm^2 HBT's and a 4 μm metalization pitch.

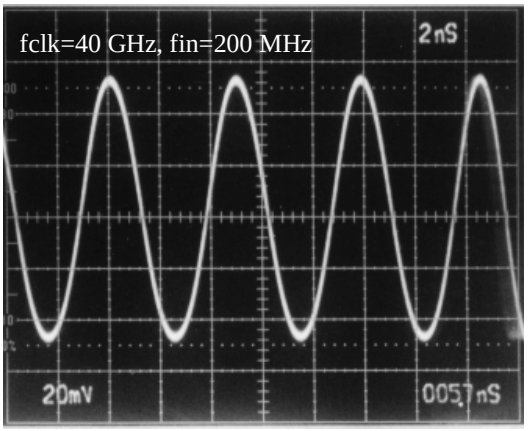

Fig. 6 output of comparator test chip driving a 25 ohm load. Clock is at 40 GHz and analog input is at 200 MHz.

V. Circuit Performance:

The comparator test chip was tested on-wafer using high-frequency probes. The testing was done up to 40 GHz, limited in part by test equipment and the probes. Several different tests

were performed on the comparator chip. In all the tests the comparator was driving an approximately 25 ohm load (50 ohm internal, parallel with a 50 ohm external load). In one test, the comparator input was held at 200 MHz while the clock frequency was increased up to 40 GHz. The comparator output signal at 40 GHz clock frequency is shown in Fig. 6. For this test, the input reference voltage was held at zero and one of the two differential outputs were measured. Changing the input reference voltage could change the duty cycle of the output signal, as expected. The frequency performance of the comparator was over 3 times that of a similar one implemented in our baseline process.

In another test, the comparator was clocked at 25 GHz with an analog input of 25100 MHz. This test condition generates a beat frequency at 100 MHz (the difference of the clock and input frequencies) as shown in Fig. 7. This test indicated that the comparator can operate at an analog input and clock frequency of both 25 GHz. Minimum device size in this comparator design was 0.5 μm^2 and the test chip consumed a total of 176 mW of dc power (supply voltage = -3.2 V, supply current = 55 mA). This was less than 1/3 of the power consumed by a similar comparator designed in our baseline process.

VI. Conclusions

A new processing approach was presented for fabricating submicron HBT's on InP substrate. The process is intended for ultra-high speed circuits with low power consumption and a very compact chip size. Excellent device dc and RF performance was achieved for devices as small as 0.3 μm^2 emitter. Circuits have been implemented in this new process. As an example a comparator test chip operating at 40 GHz was presented.

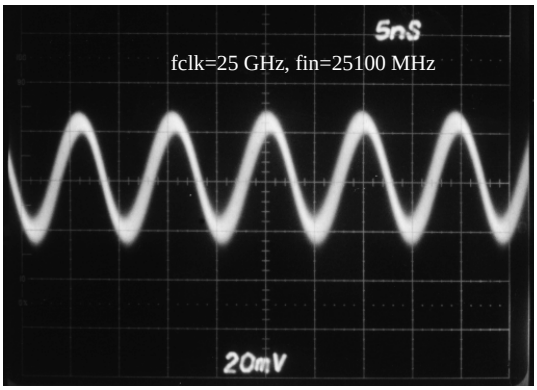

Fig. 7 Beat frequency test of comparator at clock frequency of 25

Acknowledgments

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